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63162 7590 07/19/2007 TRASK BRITT, P.C./ MICRON TECHNOLOGY P.O. BOX 2550 SALT LAKE CITY, UT 84110			EXAMINER DICKEY, THOMAS L	
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Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

# Office Action Summary

Application No.

09/944,230

Applicant(s)

WHITMAN ET AL.

Examiner

Thomas L. Dickey

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-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

## Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

## Status

- 1) ☒ Responsive to communication(s) filed on 16 May 2007.
- 2a) ☐ This action is **FINAL**. 2b) ☒ This action is non-final.
- 3) ☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

## Disposition of Claims

- 4) ☒ Claim(s) 1,3,4,11,12,15,16,18-21,23 and 25-34 is/are pending in the application.
- 4a) Of the above claim(s) \_\_\_\_\_ is/are withdrawn from consideration.
- 5) ☐ Claim(s) \_\_\_\_\_ is/are allowed.
- 6) ☒ Claim(s) 1,3,4,11,12,15,16,18-21,23 and 25-34 is/are rejected.
- 7) ☐ Claim(s) \_\_\_\_\_ is/are objected to.
- 8) ☐ Claim(s) \_\_\_\_\_ are subject to restriction and/or election requirement.

## Application Papers

- 9) ☒ The specification is objected to by the Examiner.
- 10) ☒ The drawing(s) filed on 24 January 2002 and 03 November 2003 is/are: a) ☒ accepted or b) ☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

- 11) ☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

## Priority under 35 U.S.C. § 119

- 12) ☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
- a) ☐ All b) ☐ Some \* c) ☐ None of:
- ☐ Certified copies of the priority documents have been received.
  - ☐ Certified copies of the priority documents have been received in Application No. \_\_\_\_\_.
  - ☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

\* See the attached detailed Office action for a list of the certified copies not received.

## Attachment(s)

- |  |   |
|--|---|
| 1) <input checked="" type="checkbox"/> Notice of References Cited (PTO-892)                                | 4) <input type="checkbox"/> Interview Summary (PTO-413)<br>Paper No(s)/Mail Date. _____ |
| 2) <input type="checkbox"/> Notice of Draftsperson's Patent Drawing Review (PTO-948)                       | 5) <input type="checkbox"/> Notice of Informal Patent Application                       |
| 3) <input type="checkbox"/> Information Disclosure Statement(s) (PTO/SB/08)<br>Paper No(s)/Mail Date _____ | 6) <input type="checkbox"/> Other: _____  |

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## DETAILED ACTION

1. The amendment filed on 05/16/2007 has been entered.

### *Response to Arguments*

2. Applicant's arguments filed 05/07/2007 have been fully considered. They are persuasive in part but not fully persuasive.

With respect to the Examiner's 35 USC § 112 ¶ 1 rejection it is argued, at page 7 of the remarks, that "Specifically, the Office Action asserts that '[A]pplicants fail to disclose how a single material layer can substantially (i.e., approximately) fill at least one recess, while at the same time having a thickness of less than about half a depth of said at least one recess.' See Office Action, pages 4-5. However, claim 1 does not recite that the material layer within the recess has a thickness of half the depth of the recess. Rather, claim 1 recites "portions of the material layer that cover a surface of the substrate having a thickness of less than about half the depth of the at least one recess." FIGs. 2 and 5 of the as-filed specification depict embodiments of material layers 18 and 28 that both substantially fill trenches 14 and 24 and, on the surface of the substrate, have thicknesses T and T' less than about half the depths D and D' of trenches 14 and 24. See also, the as-filed Specification, paragraphs [0011], [0013], [0039], and [0043], which describe one embodiment in which the material is a mask material."

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Applicants' argument portrays an device that is different from the one the Examiner read into the claims, one to which the Examiner's 35 USC § 112 ¶ 1 rejection does not apply. One might wonder what the exact scope of the phrase, "thickness of less than about half the depth of the at least one recess" is. This phrase might restrict the claimed invention to thicknesses  $T$  (as shown in figure 2) in the range from just above 0 to just below half of  $D$  ( $D$  as shown in figure 2), i.e.  $0 < T < D/2$ . On the other hand the phrase "thickness of less than about half the depth of the at least one recess" might encompass  $0 < = T < D/2$ , so as include  $T=0$ .

It is noted that paragraph 0013, specifically cited by applicants, states: "If material of the mask covers the surface of the semiconductor substrate, the thickness of mask material thereover is significantly less than the depths of the shallow trenches.

Preferably, the thickness of mask material covering the surface of the semiconductor substrate is less than about half the depths of the trenches. More preferably, the surface [the claimed "cover[ed] surface of the substrate"] of the semiconductor substrate remains substantially uncovered [emphasis added] by the mask material." Thus it is clear that Applicants intend the claim phrase, "portions of the material layer that cover a surface of the substrate having a thickness of less than about half a depth of the at least one recess," to include an embodiment (such as is shown in Applicants' figure 3) where

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$T=0$ , i.e., where the claimed "material layer" simply does not extend over the "covered" surface of the substrate.

In paragraph 0039 (also specifically cited by applicants) the application-as-filed defines the invention with the words (referencing figure 2): "The thickness  $T$  of portions of mask layer 18 overlying surface 12 is less than the depth  $D$  of containers 14 and, preferably, is less than about half of depth  $D$ ." It appears that at the time of filing applicants envisioned an invention involving a mask layer that might not extend over the extended flat surface 12 at all (paragraph 0013) but if it did, would not be too much thicker, over said extended surface 12, than the depth  $D$  of containers 14. In paragraph 0042 the application-as-filed continues, "Referring now to FIG. 3, once a mask layer 18 with a substantially planar surface 19 is formed, the portions of mask layer 18 and of hemispherical grain silicon layer 16 that are located above a plane of surface 12 are removed from stacked capacitor structure 10." In other words, the application-as-filed teaches a material layer that fills a recess and thinly (paragraph 0039) covers a surface of a substrate, perhaps (paragraph 0013) even leaving portions of the substrate uncovered, and that is in any event ultimately completely removed (paragraph 0042;

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see also figure 3) from said surface. To borrow a phrase from Justice Scalia<sup>1</sup>, "Gee, there's less [literally less and less and less, as Applicants remove both material layer 18 (fig. 2) and intermediate layer 16 (fig. 2) from the surface of substrate 15 (figs. 2,3) to fully expose substrate 15, as shown in figure 3] here than meets the eye." Given that the invention contemplates, as a final step, the complete removal of the material layer, Applicant's comments<sup>2</sup> regarding how thin the material layer gets while it is in the process of being removed sound more like observations than inventions. Nevertheless, and in the spirit of things, the Examiner has attempted to find art that explicitly disclosed (or at least would have suggested) at the time of the invention, how thin a layer could have gotten whilst one was planing it completely away. This paper is non-final in view of the newly cited art.

It is argued, at page 8 of the remarks, that "Regarding claim 34, it is respectfully submitted that the as-filed specification provides support for the recitation of at least one valley forming a remaining portion of at least one recess. Specifically, FIG. 1 of the as-filed specification shows an embodiment in which a valley lies both partially in and

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<sup>1</sup> Oral Arguments, *MedImmune v. Genentech* (Supreme Court 2006, 05-608), argued 10/04/06. See page 22 of the transcript posted at: [http://www.supremecourtus.gov/oral\\_arguments/argument\\_transcripts/05-608.pdf](http://www.supremecourtus.gov/oral_arguments/argument_transcripts/05-608.pdf)

<sup>2</sup> "The thickness T of portions of mask layer 18 overlying surface 12 is less than the depth D of containers 14 and, preferably, is less than about half of depth D." Paragraph 0039.

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substantially above a recess. As such, it is respectfully submitted that claim 34 complies with the written description requirement of the first paragraph of 35 U.S.C. § 112."

However, FIG. 1 of the as-filed specification has been clearly marked "prior art" since the initial filing of this application. Applicants are not allowed, at this late date, to appropriate aspects of the prior art as part of their own invention.

***Claim Rejections - 35 USC § 112***

3. The following is a quotation of the first paragraph of 35 U.S.C. 112:

The specification shall contain a written description of the invention, and of the manner and process of making and using it, in such full, clear, concise, and exact terms as to enable any person skilled in the art to which it pertains, or with which it is most nearly connected, to make and use the same and shall set forth the best mode contemplated by the inventor of carrying out his invention.

Claims 16 and 34 are rejected under 35 U.S.C. 112, first paragraph, as failing to comply with the written description requirement. The claim(s) contains subject matter which was not described in the specification in such a way as to reasonably convey to one skilled in the relevant art that the inventor(s), at the time the application was filed, had possession of the claimed invention. Claim 16, which depends from claim 15, requires a material layer to substantially fill a valley located substantially above a recess included in a substrate, while covering (note Applicant's 5/7/07 remarks, cited above) an intermediate layer that in its turn covers the substrate. At the same time claim 16 requires said material layer to expose at least one region of the substrate. The

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application as filed discloses valley-filling, intermediate layer-covering material layer 38 (which does not expose substrate 21) in figure 7. Separately, the application as filed discloses regions of substrate 21 exposed through intermediate layer 38' in figure 10. In figure 10, however, there is no valley for intermediate layer 38' to fill. In no event does the application as filed teach that said substrate may be exposed through said material layer at the same time that said material layer fills a valley and covers an intermediate layer with a thickness of less than half the thickness of said valley.

Furthermore claim 34, which requires at least one valley to be located partially within at least one recess that is included in a substrate, is not taught by the application as filed. The particular placement (cited as new matter) of the claim 34 valley is mentioned as a feature of the prior art, as applicants point out in their 5/7/07 remarks, referring to "prior art" figure 1. But the admitted prior art valley of prior art figure 1 does not disclose claim 34 because it is not substantially filled with a "material layer having a substantially planar surface, the material layer covering a surface of the intermediate layer having a thickness of less than about half a depth of the at least one valley," as is required of the claim 34 valley.



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***Claim Rejections - 35 USC § 103***

4. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negated by the manner in which the invention was made.

A. Claims 1,3,11,12, and 21 are rejected under 35 U.S.C. 103(a) as being unpatentable over KIKUCHI ET AL. (6,278,153) in view of YOSHIHARA (6,117,486).

In Ex parte JOHN WHITMAN and JOHN DAVLIN, Appeal No. 2006-1362, Application No. 09/542,783, decided July 25, 2006, Applicants presented a claim (claim 1) to the Board of Patent Appeals and Interferences, which recited, inter alia:

1. A method ... comprising: providing a semiconductor device structure including a surface and at least one recess formed in said surface; disposing [a] material on said surface so as to substantially fill said at least one recess, said material covering said surface having a thickness less than a depth of said at least one recess ... an upper surface of at least a portion of said material ... being substantially planar.

*Ex parte* WHITMAN at 2. The Board rejected this claim under a new ground of rejection using its authority under 37 CFR § 41.50(b). Id at 12. The said claim 1 was rejected under 35 U.S.C. § 103(a) as being unpatentable over the collective teachings of Kikuchi and Yoshihara. The Board explained, "In our affirmance of the rejection of claim 3 above, we explained how the collective teachings of Kikuchi and Yoshihara render the invention of claim 3 obvious. Since claim 3 depends from claim 1, then claim

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1 is unpatentable over the teachings of Kikuchi and Yoshihara for the same reasons discussed above with respect to claim 3. As discussed above, only Yoshihara teaches the formation of a substantially planar layer. Therefore, on this record, only rejections which rely on Yoshihara can support a finding of a substantially planar surface."

It has been held that general principles of collateral estoppel should apply to bar reconsideration of questions of fact or mixed questions of fact and law which form the basis for a judgment previously rendered by the Board, if those questions of fact or mixed questions of fact and law were resolved in the earlier litigation. See *In re Pritchard*, 43 F.2d 1359, 175 USPQ 17, 21 (CCPA 1972) (citing *Yates v. United States*, 354 U.S. 298, 335-38 (1957); *Partmar Corp. v. Paramount Corp.*, 347 U.S. 89, 90-91 (1954); and *Commissioner v. Sunnen*, 333 U.S. 591, 597-602, 77 USPQ 29, 31-33 (1948)). An estoppel of this sort is invoked for various reasons of judicial and public policy. *Id.* Regardless of whether the Examiner is actually bound by findings of the Board in the prior case, he finds them highly persuasive. It is noted that the previous claim 1 and the present (amended) claim 1 differ as to form, and as to their precise scope (previous claim 1 is broader).

The present claim 1 claims a device having a surface and at least one recess formed in said surface and a material disposed on said surface so as to substantially fill said at least one recess, said material covering said surface having a thickness (T) less

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than a depth (D) of said at least one recess an upper surface of at least a portion of said material ... being substantially planar. It is clear that such a device is the necessary product of the step of disposing the material presently claimed in the manner the presently claimed material is claimed to be disposed, over the presently claimed substrate (as provided by a step of the previous claim). Note Figs. 6A-6D; 10A-10E and 13A-13E of Kikuchi et al. and Figs. 10 and Col. 13, lines 25- 44 of Yoshihara.

The difference between the present claim and the necessary product of the method so clearly (in the Board's view) obvious over Kikuchi et al. in view of Yoshihara is that the present claim requires the material layer have a thickness (T) in the range from 0 to  $.5 \cdot D$  (D being the depth (D)), whereas in the claimed device previously found to be an obvious (in view of Yoshihara) variation of the Kikuchi et al. device, the thickness (T) of the material layer was allowed a larger range, namely from 0 to D.

Furthermore, re claims 11-12, as applied to claim 1 above, Kikuchi et al. and Yoshihara in combination disclose all the claimed limitations including the limitation wherein said semiconductor device structure so provided comprises a stacked capacitor structure, with the at least one recess comprising at least one container recessed in an insulator layer of said stacked capacitor structure, wherein said material layer comprises a mask material, said mask material substantially filling said at least one container, and wherein mask material covering a surface of said insulator layer has a thickness of less

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than about half a depth of said at least one container. See Figs. 6A-6D; 10A-10E; 13A-13E. Re claims 3 and 21 as applied to claim 1 above, Kikuchi et al. and Yoshihara in combination disclose all the claimed limitations including the limitation wherein said disposed material comprises a mask material over said semiconductor device structure, and the surface of the material layer is free of abrasive-planarization-induced defects. See Fig. 6A-6D; 10A-10E; 13A-13E.

Kikuchi et al. and Yoshihara thus suggest a device having all limitations of the claimed device, except that Applicant's claimed material layer thickness range of 0 to  $.5 \cdot D$  (again,  $D$  being the depth of the recess) lies within the disclosed range of 0 to  $D$  for the prior art.

The Federal Circuit informs us that a prima facie case of obviousness typically exists when the ranges of a claimed composition overlap the ranges disclosed in the prior art. *In re Peterson*, 65 USPQ2d 1379, 1382 (Fed. Cir. 2003) citing *In re Geisler*, 116 F.3d 1465, 1469, 43 USPQ2d 1362, 1365 (Fed. Cir. 1997); *In re Woodruff*, 919 F.2d 1575, 1578, 16 USPQ2d 1934, 1936-37 (CCPA 1976); and *In re Malagari*, 499 F.2d 1297, 1303, 182 USPQ 549, 553 (CCPA 1974). See MPEP § 2144.05.

It is well understood that obviousness based upon a combination of elements requires a suggestion, motivation or teaching to those skilled in the art for such a combination. *In re Fine*, 5 USPQ2d 1596 (Fed. Cir. 1988). This requirement prevents

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the use of “the inventor’s disclosure as a blueprint for piecing together the prior art to defeat patentability—the essence of hindsight.” *Ecolochem, Inc. v. So. Cal. Edison Co.*, 56 USPQ2d 1065 (Fed. Cir. 2000) (quoting *In re Dembiczak*, 50 USPQ2d 1614 (Fed. Cir. 1999)). However, as the Federal Circuit points out in *Iron Grip Barbell Co. v. USA Sports Inc.*, when the difference between the claimed invention and the prior art rests only in the fact that applicants claim a narrower range than that found in the prior art, the case for obviousness does not rest on combining elements, and evidence of motivation/suggestion is not required to avoid using hindsight. *Iron Grip Barbell Co. v. USA Sports Inc.*, 73 USPQ2d 1225, 1227 (Fed. Cir. 2004). Iron Grip also teaches us that whether the prior art range is found in one, two, or many references is “a distinction without a difference.” *Id* at 1228. See also MPEP § 2144.05.

Therefore the fact that applicant’s claimed range overlaps the prior art range establishes a presumption of obviousness. This presumption may be rebutted when Applicants puts forward evidence demonstrating objective indicia of non-obviousness, e.g. that the prior art taught away from the claimed invention, *In re Geisler*, 43 USPQ2d 1362 (Fed. Cir. 1997); or that there are new and unexpected results relative to the prior art, *In re Woodruff*, 16 USPQ2d 1934 (Fed. Cir. 1990). See MPEP § 716.02(d); *Iron Grip* at 1228.

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**B.** Claim 4 stands rejected under 35 U.S.C. 103(a) as being unpatentable over KIKUCHI ET AL. (6,278,153) in view of YOSHIHARA (6,117,486), as applied to claim 3 above, and further in view of DENNISON et al. (5,663,090).

Kikuchi et al. and Yoshihara suggest a semiconductor device structure with all the limitations of claim 4 except that the substrate include at least one conductively doped region continuous with a surface of the semiconductor substrate and adjacent the at least one recess. Note Figs. 6A-6D; 10A-10E and 13A-13E of Kikuchi et al. and Figs. 10 and Col. 13, lines 25- 44 of Yoshihara.

However, Dennison et al. discloses a semiconductor device structure with substrate 40 including at least one conductively doped region 41 that is adjacent to a recess (the recess being filled with lower electrode 43 of a stacked capacitor structure. Note figure 4b of Dennison et al. Therefore, it would have been obvious to a person having skill in the art to replace the substrate of Kikuchi et al.'s semiconductor device structure with the substrate including at least one conductively doped region that is adjacent a recess containing a stacked capacitor structure, such as taught by Dennison et al. in order to utilize the semiconductor device structure of Kikuchi et al. alongside a MOSFET such as taught by Dennison et al. to thus utilize the semiconductor device structure of Kikuchi et al. as the capacitor of a DRAM memory.

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C. Claims 15, 18-20, 23, and 27-33 are rejected under 35 U.S.C. 103(a) as being unpatentable over PARK ET AL. (2002/0137279).

With respect to claims 28-32 Park et al. discloses a semiconductor device structure, comprising a substrate 100-102-103-104 including at least one peak (seen in figures 2B-C on either side of recess 110, and again, in figure 2E, on either side of said recess 110) exposed through an intermediate layer 112, at least one peak also being exposed through a material layer 116-118 (note figure 2E, material layer 116-118 has been planarized very thinly by this time. Also, at least one peak of the intermediate layer 112 is exposed through the material layer 116-118 at this time), and at least one recess 110 formed therein; intermediate layer 112 filling a portion of the at least one recess 110 and leaving at least portions (said peaks) of a surface of the substrate 100-102-103-104 exposed through the intermediate layer 112; and a material layer 116-118 disposed over the intermediate layer 112 and substantially filling a remaining portion of the at least one recess 110, the material layer 116-118 having a substantially planar surface. Note figures 2D, 2E, and paragraphs 0025-0032 of Park et al.

Park et al. do not explicitly disclose any particular thickness for their material layer 116-118; in fact, at any given time, the precise thickness of their material layer seems to be a matter of indifference to Park et al., as it might be to anyone who, like Park et al. (or Applicants, for that matter) intends to planarize said material layer until it altogether

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disappears. Therefore Park et al. do not explicitly disclose that the portion of their material layer 116-118 covering a surface of the intermediate layer 112 has a thickness of less than about half a depth of the remaining portion of the at least one recess 110. What Park et al. do explicitly (paragraph 0029) disclose is that a planarization process is performed on the material layer 116-118 of figure 2D (which initially may or may not have a thickness of less than about half a depth of the remaining portion; the reader has no way of knowing), and at the end of that process, the relevant thickness of material layer 116-118 is zero (which is definitely less than half a depth of any possible remaining portion, however, to briefly indulge Applicants the Examiner will assume that a thickness of zero does not meet Applicants' claims).

It has been previously explained to Applicants that:

In rejecting claims under 35 U.S.C. 103, it is incumbent upon the examiner to establish a factual basis to support the legal conclusion of obviousness. See *In re Fine*, 837 F.2d 1071, 1073, 5 USPQ2d 1596, 1598 (Fed. Cir. 1988). In so doing, the examiner is expected to make the factual determinations set forth in *Graham v. John Deere Co.*, 383 U.S. 1, 17, 148 USPQ 459, 467 (1966). The examiner must articulate reasons for the examiner's decision. *In re Lee*, 27F.3d 1338, 1342, 61 USPQ2d 1430, 1434 (Fed. Cir. 2002). In particular, the examiner must show that there is a teaching, motivation, or suggestion of a motivation to combine references relied on as evidence of obviousness. *Id.* at 1343, 61 USPQ2d at 1433-34. The examiner cannot simply reach conclusions based on the examiner's own understanding or experience - or on his or her assessment of what would be basic knowledge or common sense. Rather, the examiner must point to some concrete evidence in the record in support of these findings. *In re Zurko*, 258 F.3d 1379, 1386, 59 USPQ2d 1693, 1697 (Fed. Cir. 2001). Thus the examiner must not only assure that the requisite findings are made, based on evidence of record, but must also explain the reasoning by which the findings are deemed to support the examiner's conclusion. However, a suggestion, teaching, or motivation to combine the relevant prior art teachings does not have to be found explicitly in the prior art, as the teaching, motivation, or suggestion may be implicit from the prior art as a whole, rather than expressly stated in the references. The test for an implicit showing is what the combined teachings, knowledge of one of ordinary skill in the art, and the nature of the problem to be solved as a whole would have suggested to those of ordinary skill in the art. *In re Kahn*, 441 F.3d 977, 987, 78 USPQ2d 1329, 1336 (Fed. Cir. 2006) (citing *In re Kotzab*, 217



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F.3d 1365, 1370, 55 USPQ2d 1313 (Fed. Cir. 2000)). See also *In re Thrift*, 298 F3d 1357, 1363, 63 USPQ2d 2002, 2008 (Fed. Cir. 2002).

*Ex parte* JOHN WHITMAN and JOHN DAVLIN, Appeal No. 2006-1362, Application No. 09/542,783, decided July 25, 2006. See also *Alza Corp. v. Mylan Labs*, 464 F.3d 1286, 1291, 80 USPQ2d 1001, 1005 (2006) ("There is flexibility in our obviousness jurisprudence because a motivation may be found implicitly in the prior art").

Furthermore, said implicit showing is not to be arrived at in a rigid, formalistic fashion.

"The obviousness analysis cannot be confined by a formalistic conception of the words teaching, suggestion, and motivation, or by overemphasis on the importance of published articles and the explicit content of issued patents. The diversity of inventive pursuits and of modern technology counsels against limiting the analysis in this way."

*KSR Int'l Co. v. Teleflex Inc.*, 82 USPQ2d 1385, 1396 (U.S. 2007). One of ordinary skill in the art is not to be considered as an automaton, but as a person of ordinary creativity, capable of drawing reasonable inferences from the prior art set before him. *Id.* at 1397.

As our own Board of Appeals explains it, "we can account for 'the inferences and creative steps that a person of ordinary skill in the art would employ.'" *Ex parte* JOAN C. TENG and THOMAS B. REMAHL, Appeal 2007-0954, Application 09/999,074, decided May 10, 2007, (citing *KSR Int'l Co. v. Teleflex Inc.*, No. 04-1350, slip op. at 14 (U.S., Apr. 30, 2007)).

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It would have been obvious to a person having skill in the art that whilst said person having skill in the art was building a semiconductor device structure according to Park et al.'s instructions, at some point during the processing of a material layer like Park et al.'s material layer 116-118 (the laying down of said layer, the planarizing of it, and the continued planarizing of it until it disappeared, as Park et al. teach) by, the thickness of said material layer would become less than about half a depth of the remaining portion thus achieving the claimed invention. The Examiner explicitly states that the reason (See *KSR International Co. v. Teleflex Inc.*, 550 U. S. \_\_ (2007), slip op. at 14) this is so is because said person having skill in the art would have been "a person of ordinary creativity, capable of drawing reasonable inferences from the prior art set before him," and that recognizing that a planarized layer gets thinner, and thinner and thinner, indefinitely, as one planarizes it completely away, is one<sup>3</sup> of said "reasonable inferences."

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<sup>3</sup> In the Examiner's opinion, the "reasonable inference" needed to realize the instant invention is a perfect example of what the KSR Court was talking about. "Ordinary Creativity" does not mean PHOSITA necessarily would have been capable of painting the Sistine Chapel – it means PHOSITA would have been capable of recognizing his own hat lying on a store counter after he had put it there, if a salesman had offered to sell PHOSITA said hat. Pre-KSR, some might have argued that PHOSITA was the sort of fellow who would have needed a little booklet titled, "How to Recognize Your Hat."

The Examiner's opinion is not controlling, of course. There will be more case law (like *Ex Parte Teng*, cited above) interpreting the KSR Court's meaning, in a few months.

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With respect to claims 15, 18-20, 23, 27, and 33 Park et al. discloses a semiconductor device structure comprising a substrate 100-102-103-104 including at least one recess 110 formed therein; an intermediate layer 116 filling at least a portion of the at least one recess 110 and covering a surface of the semiconductor device substrate 100-102-103-104, the intermediate layer 116 including at least one valley (seen as a dip or depression in the surface of intermediate layer 116, directly above recess 110) located substantially above the at least one recess 110; and a material layer 118 disposed over the intermediate layer 116 and substantially filling the at least one valley, the material layer 118 having a substantially planar surface. With particular regard to claims 15, 18-20, 23, and 27, Park et al. discloses that the filling of at least a portion of the at least one recess 110 results in the substantial filling thereof. Park et al. also discloses, with respect to claims 19, 23, and 27, that the intermediate layer 116 comprises an insulative material and the material layer 118 comprises a stress buffer layer with an abrasive-planarization-induced defect free surface. Note figures 2D, 2E, and paragraphs 0025-0032 of Park et al.

Park et al. do not explicitly disclose any particular thickness for their material layer 118; in fact, at any given time, the precise thickness of their material layer seems to be a matter of indifference to Park et al., as it might be to anyone who, like Park et al. (or Applicants, for that matter) intends to planarize said material layer until it altogether

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disappears. Therefore Park et al. do not explicitly disclose that their material layer 118 (or portions thereof, as claimed in claims 15, 18-20, 23, and 27) covering a surface of the intermediate layer 116 has a thickness of less than about half a depth of the at least one valley (or less than a depth of recess 110, as claimed in claim 20), or that a region of intermediate layer 116 is exposed through material layer 118, as claimed in claim 18. What Park et al. do explicitly (paragraph 0029) disclose is that a planarization process is performed on the material layer 118 of figure 2D (which initially may or may not have a thickness of less than about half a depth of the remaining portion; the reader has no way of knowing), and at the end of that process, material layer 118 is completely and utterly gone (compare figure 2E to 2D) the relevant thickness of material layer 118 is zero (which is definitely less than half a depth of the at least one valley, however, to briefly indulge Applicants the Examiner will assume that a thickness of zero does not meet Applicants' claims).

It has been previously explained to Applicants that:

In rejecting claims under 35 U.S.C. 103, it is incumbent upon the examiner to establish a factual basis to support the legal conclusion of obviousness. See *In re Fine*, 837 F.2d 1071, 1073, 5 USPQ2d 1596, 1598 (Fed. Cir. 1988). In so doing, the examiner is expected to make the factual determinations set forth in *Graham v. John Deere Co.*, 383 U.S. 1, 17, 148 USPQ 459, 467 (1966). The examiner must articulate reasons for the examiner's decision. *In re Lee*, 27F.3d 1338, 1342, 61 USPQ2d 1430, 1434 (Fed. Cir. 2002). In particular, the examiner must show that there is a teaching, motivation, or suggestion of a motivation to combine references relied on as evidence of obviousness. *Id.* at 1343, 61 USPQ2d at 1433-34. The examiner cannot simply reach conclusions based on the examiner's own understanding or experience - or on his or her assessment of what would be basic knowledge or common sense. Rather, the examiner must point to some concrete evidence in the record in support of these findings. *In re Zurko*, 258 F.3d 1379, 1386, 59 USPQ2d 1693, 1697 (Fed. Cir. 2001). Thus the

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examiner must not only assure that the requisite findings are made, based on evidence of record, but must also explain the reasoning by which the findings are deemed to support the examiner's conclusion. However, a suggestion, teaching, or motivation to combine the relevant prior art teachings does not have to be found explicitly in the prior art, as the teaching, motivation, or suggestion may be implicit from the prior art as a whole, rather than expressly stated in the references. The test for an implicit showing is what the combined teachings, knowledge of one of ordinary skill in the art, and the nature of the problem to be solved as a whole would have suggested to those of ordinary skill in the art. *In re Kahn*, 441 F.3d 977, 987, 78 USPQ2d 1329, 1336 (Fed. Cir. 2006) (citing *In re Kotzab*, 217 F.3d 1365, 1370, 55 USPQ2d 1313 (Fed. Cir. 2000)). See also *In re Thrift*, 298 F3d 1357, 1363, 63 USPQ2d 2002, 2008 (Fed. Cir. 2002).

*Ex parte* JOHN WHITMAN and JOHN DAVLIN, Appeal No. 2006-1362, Application No. 09/542,783, decided July 25, 2006. See also *Alza Corp. v. Mylan Labs*, 464 F.3d 1286, 1291, 80 USPQ2d 1001, 1005 (2006) ("There is flexibility in our obviousness jurisprudence because a motivation may be found implicitly in the prior art"). Furthermore, said implicit showing is not to be arrived at in a rigid, formalistic fashion. "The obviousness analysis cannot be confined by a formalistic conception of the words teaching, suggestion, and motivation, or by overemphasis on the importance of published articles and the explicit content of issued patents. The diversity of inventive pursuits and of modern technology counsels against limiting the analysis in this way." *KSR Int'l Co. v. Teleflex Inc.*, 550 U. S. \_\_\_, 82 USPQ2d 1385, 1396 (U.S. 2007). One of ordinary skill in the art is not to be considered as an automaton, but as a person of ordinary creativity, capable of drawing reasonable inferences from the prior art set before him. *Id.* at 1397. As our own Board of Appeals explains it, "we can account for 'the inferences and creative steps that a person of ordinary skill in the art would employ.'" *Ex parte* JOAN C. TENG and THOMAS B. REMAHL, Appeal 2007-0954,

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Application 09/999,074, decided May 10, 2007, (citing *KSR Int'l Co. v. Teleflex Inc.*, No. 04-1350, slip op. at 14 (U.S., Apr. 30, 2007)).

It would have been obvious to a person having skill in the art that whilst said person having skill in the art was building a semiconductor device structure according to Park et al.'s instructions, at some point during the processing of a material layer like Park et al.'s material layer 118 (the laying down of said layer, the planarizing of it, and the continued planarizing of it until it disappeared, as Park et al. teach) by, the thickness of said material layer would become less than about half a depth of the remaining portion thus achieving the claimed invention. With regard to claim 18, it would likewise have been obvious to said person having skill in the art that although intermediate layer 116 is not explicitly exposed in Park et al.'s drawings and description, the steady planarizing removal of material layer 118 would, at some point, expose it. With regard to claim 20, It would likewise have been obvious to said person having skill in the art that although Applicant's goal of reducing material layer thickness to the depth of recess 110 is not explicitly achieved in Park et al.'s drawings and description, the steady planarizing removal of material layer 118 would, at some point, achieve it. The Examiner explicitly states that the reason (See *KSR*, 550 U. S. at \_\_\_, 82 USPQ2d at 1396) this is so is because said person having skill in the art would have been "a person of ordinary creativity, capable of drawing reasonable inferences from the prior art set before him,"

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(*Id.* at 1395) and that recognizing that a planarized layer gets thinner and thinner and thinner, indefinitely, as one planarizes it completely away, is one of said "reasonable inferences" (*Id.*).

The Examiner also believes that the logic of Heller's Paradox, known as "Catch-22," may be combined with the legal principle set forth in *Iron Grip*, to render claims 15, 18-20, 23, and 27-33 necessarily either anticipated by Park et al. or per se obvious (under *Woodruff-Geisler-Peterson-Iron Grip*) in view of Park et al.

Park et al. discloses a material layer having thicknesses falling in a range from zero to an unknown maximum. It cannot be said that this unknown maximum is small enough so that Park et al.'s range anticipates Applicant's claimed range. But by showing that the disclosed range fails to anticipate, on the grounds that the top of the disclosed range is greater than the top of the claimed range, the investigator demonstrates that the claimed range is in fact overlapped by the disclosed range and therefore *per se* obvious in view thereof. See *Iron Grip*, 73 USPQ2d at 1227, *In re Geisler*, 43 USPQ2d 1362 (Fed. Cir. 1997); *In re Woodruff*, 16 USPQ2d 1934 (Fed. Cir. 1990). See also MPEP § 716.02(d). One might argue, of course, that proof that the claims cannot legally be rejected as anticipated if they might be *per se* obvious, and that they cannot be rejected as *per se* obvious if they might be anticipated. Such an argument clearly parallels the following "logic," however:

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Orr was crazy and could be grounded. All he had to do was ask; and as soon as he did, he would no longer be crazy and would have to fly more missions. Orr would be crazy to fly more missions and sane if he didn't, but if he was sane he had to fly them. If he flew them he was crazy and didn't have to; but if he didn't want to he was sane and had to. Yossarian was moved very deeply by the absolute simplicity of this clause of Catch-22 and let out a respectful whistle.

Heller, Joseph, *Catch-22, a Novel*, New York, Simon and Schuster, 1961.

D. Claims 15, 18-20, 23, and 27-33 are rejected under 35 U.S.C. 103(a) as being unpatentable over WANG (6,461,932).

With respect to claims 15, 18-20, 23, 25, and 26 Wang discloses a semiconductor device structure comprising a substrate 40-42-44 including at least one recess 54 formed therein; an intermediate layer 56 including a nonplanar upper surface with at least one peak 58 located substantially above the surface of the semiconductor device substrate and at least one valley (the several "dips" in layer 56 seen in figure 4d, directly above the recesses 54) located substantially above the at least one recess, the intermediate layer 56 substantially filling the at least one recess 54 and covering a surface of the semiconductor device substrate 40-42-44, and a material layer 60 disposed over the intermediate layer 56 and substantially filling the at least one valley, the material layer 60 having a substantially planar surface 62. Wang also discloses, with respect to claims 19, 23, and 26, that the intermediate layer 56 comprises an insulative material and the material layer 60 comprises a mask layer with an abrasive-planarization-induced defect free surface. Note figures 4D, 4E, column 6 lines 14-64, column 7 lines 42-67, and column 8 lines 1-16 of Wang.



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Wang do not explicitly disclose any particular thickness for his material layer 60; in fact at any particular point in time the precise thickness of his material layer seems to be a matter of indifference to Wang, as it might be to anyone who, like Wang (or Park et al., or Applicants, for that matter) intends to planarize said material layer until it altogether disappears. Therefore Wang do not explicitly disclose that his material layer 60 (or portions thereof, as claimed in claims 15, 18-20, 23, and 27) covering a surface of the intermediate layer 56 has a thickness of less than about half a depth of the at least one valley (or less than a depth of recess 54, as claimed in claim 20), or that a region of intermediate layer 56 is exposed through material layer 60, as claimed in claim 18. What Wang does explicitly (column 7 lines 44-53) disclose is that a planarization process is performed on the material layer 60 of figure 2D (which initially may or may not have a thickness of less than about half a depth of the remaining portion; the reader has no way of knowing), and at the end of that process, material layer 60 is completely and utterly gone (compare figure 4E to 4D) the relevant thickness of material layer 60 is zero (which is definitely less than half a depth of the at least one valley, however, to briefly indulge Applicants the Examiner will assume that a thickness of zero does not meet Applicants' claims).

As Applicants are no doubt aware:

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In rejecting claims under 35 U.S.C. 103, it is incumbent upon the examiner to establish a factual basis to support the legal conclusion of obviousness. See *In re Fine*, 837 F.2d 1071, 1073, 5 USPQ2d 1596, 1598 (Fed. Cir. 1988). In so doing, the examiner is expected to make the factual determinations set forth in *Graham v. John Deere Co.*, 383 U.S. 1, 17, 148 USPQ 459, 467 (1966). The examiner must articulate reasons for the examiner's decision. *In re Lee*, 27F.3d 1338, 1342, 61 USPQ2d 1430, 1434 (Fed. Cir. 2002). In particular, the examiner must show that there is a teaching, motivation, or suggestion of a motivation to combine references relied on as evidence of obviousness. *Id.* at 1343, 61 USPQ2d at 1433-34. The examiner cannot simply reach conclusions based on the examiner's own understanding or experience - or on his or her assessment of what would be basic knowledge or common sense. Rather, the examiner must point to some concrete evidence in the record in support of these findings. *In re Zurko*, 258 F.3d 1379, 1386, 59 USPQ2d 1693, 1697 (Fed. Cir. 2001). Thus the examiner must not only assure that the requisite findings are made, based on evidence of record, but must also explain the reasoning by which the findings are deemed to support the examiner's conclusion. However, a suggestion, teaching, or motivation to combine the relevant prior art teachings does not have to be found explicitly in the prior art, as the teaching, motivation, or suggestion may be implicit from the prior art as a whole, rather than expressly stated in the references. The test for an implicit showing is what the combined teachings, knowledge of one of ordinary skill in the art, and the nature of the problem to be solved as a whole would have suggested to those of ordinary skill in the art. *In re Kahn*, 441 F.3d 977, 987, 78 USPQ2d 1329, 1336 (Fed. Cir. 2006) (citing *In re Kotzab*, 217 F.3d 1365, 1370, 55 USPQ2d 1313 (Fed. Cir. 2000)). See also *In re Thrift*, 298 F.3d 1357, 1363, 63 USPQ2d 2002, 2008 (Fed. Cir. 2002).

*Ex parte* JOHN WHITMAN and JOHN DAVLIN, Appeal No. 2006-1362, Application No. 09/542,783, decided July 25, 2006. See also *Alza Corp. v. Mylan Labs*, 464 F.3d 1286, 1291, 80 USPQ2d 1001, 1005 (2006) ("There is flexibility in our obviousness jurisprudence because a motivation may be found implicitly in the prior art").

Furthermore, said implicit showing is not to be arrived at in a rigid, formalistic fashion.

"The obviousness analysis cannot be confined by a formalistic conception of the words

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teaching, suggestion, and motivation, or by overemphasis on the importance of published articles and the explicit content of issued patents. The diversity of inventive pursuits and of modern technology counsels against limiting the analysis in this way." *KSR Int'l Co. v. Teleflex Inc.*, 550 U. S. \_\_\_, 82 USPQ2d 1385, 1396 (U.S. 2007). One of ordinary skill in the art is not to be considered as an automaton, but as a person of ordinary creativity, capable of drawing reasonable inferences from the prior art set before him. *Id.* at 1397. As our own Board of Appeals explains it, "we can account for 'the inferences and creative steps that a person of ordinary skill in the art would employ.'" *Ex parte* JOAN C. TENG and THOMAS B. REMAHL, Appeal 2007-0954, Application 09/999,074, decided May 10, 2007, (citing *KSR Int'l Co. v. Teleflex Inc.*, No. 04-1350, slip op. at 14 (U.S., Apr. 30, 2007)).

It would have been obvious to a person having skill in the art that whilst said person having skill in the art was building a semiconductor device structure according to Wang's instructions, at some point during the processing of a material layer like Wang's material layer 60 (the laying down of said layer, the planarizing of it, and the continued planarizing of it until it disappeared, as Wang teach) by, the thickness of said material layer would become less than about half a depth of the remaining portion thus achieving the claimed invention. With regard to claim 18, it would likewise have been obvious to said person having skill in the art that although intermediate layer 56 is not explicitly

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exposed in Wang's drawings and description, the steady planarizing removal of material layer 60 would, at some point, expose it. With regard to claim 20, It would likewise have been obvious to said person having skill in the art that although Applicant's goal of reducing material layer 60's thickness to the depth of recess 54 is not explicitly achieved in Wang's drawings and description, the steady planarizing removal of material layer 60 would, at some point, achieve it. The Examiner explicitly states that the reason (See *KSR*, 550 U. S. at \_\_\_, 82 USPQ2d at 1396) this is so is because said person having skill in the art would have been "a person of ordinary creativity, capable of drawing reasonable inferences from the prior art set before him," (*Id.* at 1395) and that recognizing that a planarized layer gets thinner and thinner and thinner, indefinitely, as one planarizes it completely away, is one of said "reasonable inferences" (*Id.*).

Heller's Paradox, "Catch-22," also appears combinable here with the legal principle set forth in *Iron Grip*, to render claims 15, 18-20, 23, 25, and 26 necessarily either anticipated by Wang or per se obvious (under *Woodruff-Geisler-Peterson-Iron Grip*) in view of Wang.

Like Park et al., Wang discloses a material layer having thicknesses falling in a range from zero to an unknown maximum. It cannot be said that this unknown maximum is small enough so that Wang's range anticipates Applicants' claimed range. But by showing that the disclosed range fails to anticipate, on the grounds that the top

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of the disclosed range is greater than the top of the claimed range, the investigator demonstrates that the claimed range is in fact overlapped by the disclosed range and therefore *per se* obvious in view thereof. See *Iron Grip*, 73 USPQ2d at 1227, *In re Geisler*, 43 USPQ2d 1362 (Fed. Cir. 1997); *In re Woodruff*, 16 USPQ2d 1934 (Fed. Cir. 1990). See also MPEP § 716.02(d).

### **Conclusion**

5. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Thomas L. Dickey whose telephone number is 571-272-1913. The examiner can normally be reached on Monday-Thursday 8-6.

If attempts to reach the examiner by telephone are unsuccessful, please contact the examiner's supervisor, Sue A. Purvis, at 571-272-1236. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see <http://pair-direct.uspto.gov>. Should you

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have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

A handwritten signature in black ink, appearing to read 'Thomas L. Dickey', is positioned above the printed name.

**/Thomas L. Dickey/  
Primary Examiner  
Art Unit 2826**